1. A photolithography method comprising the steps of:

depositing a first anti-reflective coating over a reflective surface, the first coating having a first index of refraction, a first absorption, an upper surface defining a first interface, and a first thickness;

depositing a second anti-reflective coating at least partially on the upper surface of said first anti-reflective coating, the second anti-reflective coating have a second index of refraction, a second absorption, an upper surface defining a second interface, and a second thickness; and

depositing photoresist over the second coating, wherein the first index of refraction is different from the second index of refraction.

2. The method according to claim 1, wherein the first index of refraction, the first absorption, and the first thickness are chosen such that the amplitude of radiation reflected from the first interface will be approximately equal to the amplitude of radiation reflected from the second interface and the phase difference between the radiation reflected from the first interface and the second interface will be approximately 180 degrees.

3. The method according to claim 1, wherein one or more additional surfaces below the second interface are also reflective.

4. The method according to claim 3, wherein the indices of refraction, absorptions, and thicknesses of the first anti-reflective coating and second anti-

reflective coating are chosen such that the amplitudes and phase differences of radiation reflected from the first interface, second interface, and additional reflective surfaces which reside below the second interface substantially mutually cancel when combined.

5. The method according to claim 1, wherein the second anti-reflective coating is deposited on the entire upper surface of said first anti-reflective coating.

6. The method according to claim 1, wherein the photoresist is in contact with the second coating.

7. The method according to claim 1, wherein the indices of refraction, absorptions, and thicknesses of the first, second, and additional anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined.

8. The method according to claim 1, further comprising the step of depositing a dielectric material between the photoresist and the second coating.

9. The method according to claim 8, wherein the dielectric material is boro-phospho silicate glass.

10. The method according to claim 8, wherein the dielectric material is tetraethylorthosilicate.

11. The method according to claim 1, wherein the reflective surface is formed of metal.

12. The method according to claim 1, wherein the reflective surface is formed of a metal silicide.

13. The method according to claim 1, wherein the reflective surface is formed of polysilicon.

14. The method according to claim 1, wherein the reflective surface is formed of an insulator.

15. The method according to claim 1, wherein the reflective surface is formed of silicon dioxide.

16. The method according to claim 1, wherein the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0, the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

17. The method according to claim 1, further comprising exposing at least a portion of said photoresist layer to light of an appropriate wavelength to form a desired pattern in said photoresist layer.

18. A method for fabricating a memory cell, the method comprising the steps of:

providing a substrate;

forming a structure on the substrate, the structure comprising

at least two active areas in the substrate;

a gate stack between the active areas; and

a capacitor in electrical contact with one of the active areas;

depositing a first anti-reflective coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface over the structure;

depositing a second anti-reflective coating having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface at least partially on the upper surface of said first anti-reflective coating;

depositing an insulating layer over the structure; and

patterning the insulating layer using a photo-lithographic process, wherein the first index of refraction is different from the second index of refraction.

19. The method according to claim 18, wherein the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined.

20. The method according to claim 18, wherein the second anti-reflective coating is deposited on the entire upper surface of said first anti-reflective coating.

21. The method according to claim 18, wherein the first and second coatings are below the insulating layer.

22. The method according to claim 18, wherein the insulating layer comprises boro-phospho silicate glass.

23. The method according to claim 18, wherein the insulating layer is tetraethylorthosilicate.

24. The method according to claim 18, wherein the patterning step comprises forming a layer of photoresist above the insulating layer, forming a desired pattern in the photoresist layer, and etching the insulating layer to transfer the desired pattern into the insulating layer.

25. The method according to claim 24, wherein the first or second anti-reflective coating is used as an etch stop during the etching.

26. The method according to claim 18, wherein the photoresist is in contact with the second coating.

27. The method according to claim 18, wherein the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0,

the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

28. The method according to claim 18, wherein the structure is a dual DRAM cell structure comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical contact with the first active area, the second capacitor being in electrical contact with the third active area, and the second active area being in electrical contact with a bit line.

29. The method according to claim 28, wherein the capacitors are formed over the gate stacks.

30. The method according to claim 29, wherein the capacitors are container capacitors.

31. The method according to claim 28, wherein the bit line is formed over the capacitors.

32. An integrated circuit comprising:

a reflective layer having a reflective surface;

a first anti-reflective coating over the reflective surface, the first coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface; and

a second anti-reflective coating at least partially on the upper surface of said first anti-reflective coating, the second anti-reflective coating having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface, wherein the first index of refraction is different from the second index of refraction.

33. The integrated circuit according to claim 32, wherein the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined.

34. The integrated circuit according to claim 32, wherein the second antireflective coating is on the entire upper surface of said first anti-reflective coating.

35. The integrated circuit according to claim 32, wherein the material placed over the second coating is photoresist placed in contact with the second coating during the manufacturing process.

36. The integrated circuit according to claim 32, further comprising at least one additional anti-reflective coating over the first and second coatings.

37. The integrated circuit according to claim 32, further comprising a dielectric material between the photoresist and the second coating.

38. The integrated circuit according to claim 32, wherein the thickness of the first coating is approximately 40 nanometers and the thickness of the second coating is approximately 25 nanometers.

39. The integrated circuit according to claim 32, wherein the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0, the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

40. A memory cell comprising:

a structure on a substrate, the structure comprising

at least two active areas formed in the substrate;

a gate stack between the active areas; and

a capacitor in electrical contact with one of the active areas;

a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface;

a second anti-reflective coating on at least a portion of the first anti-reflective coating, the second anti-reflective coating having a second index of refraction, a

second absorption, a second thickness, and an upper surface defining a second interface; and

a patterned insulating layer over the structure, the insulating layer being patterned by a photo-lithographic process, wherein the first index of refraction is different from the second index of refraction.

41. The integrated circuit according to claim 40, wherein the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined.

42. The memory cell according to claim 40, wherein the second anti-reflective coating is formed entirely on said first anti-reflective coating.

43. The memory cell according to claim 40, wherein the first and second coatings are below the insulating layer.

44. The memory cell according to claim 40, wherein the structure is a dual DRAM cell structure comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical contact with the

first active area, the second capacitor being in electrical contact with the third active area, and the second active area being in electrical contact with a bit line.

45. The memory cell according to claim 44, wherein the capacitors are formed over the gate stacks.

46. The memory cell according to claim 45, wherein the capacitors are container capacitors.

47. The memory cell according to claim 44, wherein the bit line is formed over the capacitors.

48. The memory cell according to claim 40, wherein the thickness of the first layer is approximately 40 nanometers and the thickness of the second layer is approximately 25 nanometers.

49. The integrated circuit according to claim 40, where the first index of refraction is approximately 2.1, the second index of refraction is approximately 2.0, the first absorption is approximately 1.2, and the second absorption is approximately 0.3.

50. An integrated circuit comprising:

at least one memory cell, the memory cell comprising

a structure on a substrate, the structure comprising

at least two active areas formed in the substrate;

a gate stack between the active areas; and

a capacitor in electrical contact with one of the active areas;

a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction and a first absorption;

a second anti-reflective coating on at least a portion of the first anti-reflective coating, the second anti-reflective coating having a second index of refraction and a second absorption; and

a patterned insulating layer over the structure, the insulating layer being patterned by a photo-lithographic process, wherein the first index of refraction is different from the second index of refraction.

51. A computer system comprising:

a processor; and

a memory, the memory comprising at least one memory cell, the memory cell comprising

a structure on a substrate, the structure comprising

at least two active areas formed in the substrate;

a gate stack between the active areas; and

a capacitor in electrical contact with one of the active areas;

a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction and a first absorption;

a second anti-reflective coating formed on the first anti-reflective coating, the second anti-reflective coating having a second index of refraction and a second absorption; and

a patterned insulating layer over the structure, the insulating layer being patterned by a photo-lithographic process, wherein the first index of refraction is different from the second index of refraction.

52. A method for forming a memory cell, the method comprising the steps of:

depositing a first anti-reflective coating over a reflective surface;

depositing a second anti-reflective coating over and in contact with the first anti-reflective coating;

depositing a dielectric material over and in contact with the second anti-reflective coating; and

etching the dielectric material, using the anti-reflective coating as an etch stop.

53. The method according to claim 52, further comprising forming a patterned layer of photoresist over the dielectric material before said etching step.

54. The method according to claim 53, wherein said etching step transfers the pattern from the patterned photoresist layer to the dielectric material.

55. A computer implemented method for designing anti-reflective coating layers with desirable properties comprising:

a) modeling a first anti-reflective coating with a first index of refraction, a first absorption, and a first thickness, wherein the first thickness is slightly less than a total maximum allowable thickness for said anti-reflective coating layers based on the requirements of a desired integrated circuit fabrication process;

b) modeling a second anti-reflective coating with a second index of refraction, a second absorption, and a second thickness, wherein the first and second indices of refraction are different, and the combined thicknesses of the first and second anti-reflective coatings is approximately equal to said total maximum allowable thickness;

c) modeling the reflective properties of the anti-reflective coatings using a lithography modeling program;

d) evaluating the reflective properties of said first and second anti-reflective coatings relative to a set of desired reflective properties;

e) adjusting the thicknesses, indices of refraction, and absorptions of the anti-reflective coatings based on said evaluating step;

f) repeating steps c, d, and e to arrive at a solution for anti-reflective coating layers which provide desired reflective properties.

56. The method according to claim 60, further comprising modeling one or more additional anti-reflective coating layers, modeling the reflective properties of said additional anti-reflective layers in the lithography modeling program during all reflective modeling steps c, evaluating the reflective properties of said additional anti-reflective layers during all evaluating steps d, and adjusting the thicknesses, indices of refraction, and absorptions of said additional anti-reflective layers during all adjusting steps e.

57. The method according to claim 60, further comprising modeling one or more additional reflective layers and modeling the reflective properties of said additional reflective layers in the lithography modeling program during all reflective modeling steps c.